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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,123	11/20/2003	Zachary Steven Smith	200209692-1	9105

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EXAMINER	
MEHRMANESH, ELMIRA	
ART UNIT	PAPER NUMBER
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/718,123	SMITH ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to an amendment filed on October 23, 2006 for the application of Smith et al., for a "Systems and methods for verifying core determinacy" filed November 20, 2003.

Claims 1-25 are pending in the application.

Claims 1-25 are rejected under 35 USC § 103.

Claims 1, 6, 8-11, 14, 16-22, and 24 have been amended.

Claim Rejections - 35 USC § 101

In response to amendments to claim 16, the last rejections of claims 16-21 have been withdrawn.

Claim Rejections - 35 USC § 112

In response to amendments to claim 16, the last rejections have been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandyam et al. (U.S. Patent No. 5,928,334) in view of Safford et al. (U.S. Patent No. 7,003,691).

As per claim 1, Mandyam discloses a method for verifying core determinacy (Fig. 1), the method comprising:

extracting data stored in core model structures (Figure 1, *actual data collected from hardware under test*, and col. 3, lines 15-16);

comparing (Fig. 1, element 110) the extracted data of one modeled processor (Fig. 1, element 108, *simulator model*) core with extracted data of another modeled processor core (Fig. 1, element 104, *hardware under test*) and (col. 3, lines 13-16)

facilitating notice of an error if any mismatching data will cause core divergence (col. 3, lines 16-17)

Mandyam fails to explicitly disclose a multi-core processor.

Safford et al. teaches:

before core divergence occurs (Fig. 4, element 235), determining if any

mismatching data will cause core divergence (Fig. 4, element 240) and (col. 3, lines 13-16). Figure 2 shows that lockstep logic 130 compares outputs 112 and 122 from the processors 110 and 120, respectively, to determine if a loss of lock step (lock step error) has occurred.

multiple cores of a single processor that operates in lockstep through testing of a modeled single processor (col. 3, lines 12-22). Safford discloses of a test system 100 includes processor 110 (designated as core 0) and processor 120 (designated as core 1). The processors 110 and 120 may be implemented on a single silicon chip (col. 2, lines 51-56) and (col. 3, lines 13-16).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the Hardware verification tool for multiprocessors of Mandyam et al. in combination with the lock-step testing system of Safford et al. to effectively evaluate lock step functionality.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Mandyam et al. discloses a method for detecting synchronization violations in a multiprocessor computer system (col. 4, lines 19-35). Safford et al. discloses a method of testing of lock-step logic in a multi-core processor system (col. 2, lines 51-56). To enhance reliability, the dual core processor, or other multiple microprocessor architected computer systems, may employ lock step features (Safford, col. 1, lines 35-37) and a loss of lock step, if not promptly corrected, may cause the computer system to crash (Safford, col. 1, lines 50-51).

As per claim 2, Mandyam discloses extracting data comprises extracting data from core data storage and interconnect elements (col. 8, lines 15-20).

As per claim 3, Mandyam discloses extracting data comprises extracting data from at least one of core buffers, core caches, core queues, core state variables, core state machines, and bus values (col. 9, lines 40-47).

As per claim 4, Mandyam discloses determining comprises accessing a data structure that matches divergence results with given mismatched data (Fig. 14) and (col. 8, lines 46-49).

As per claim 5, Mandyam discloses determining comprises implementing an algorithm that uses the mismatched data as inputs (col. 10, lines 33-40).

As per claim 6, Mandyam discloses facilitating notice comprises pending a check (Fig. 13, BNE SYNC _ERROR) for a lockstep block checker to signal when divergence occurs (col. 12, lines 57-67).

Safford et al. teaches:

the lockstep block checker being configured to monitor operation of a modeled lockstep block of the modeled single processor, the modeled lockstep block being configured to monitor operation of the modeled processor cores (Fig. 2 and 3) and (col.

2, lines 51-56) and (col. 3, lines 12-22).

As per claim 7, Mandyam discloses facilitating notice comprises flagging an error (col. 9, lines 14-16) if the lockstep block checker does not signal that divergence occurred (col. 8, lines 30-45).

As per claim 8, Mandyam discloses determining if the modeled single processor is operating in lockstep mode (col. 12, lines 57-67).

As per claim 9, Mandyam discloses determining if the modeled single processor is operating in lockstep mode comprises analyzing at least one of a lockstep block and a lockstep block checker (Fig. 16).

Safford et al. teaches:

the modeled lockstep block being configured to monitor operation of the modeled processor cores and the, lockstep block checker being configured to monitor operation of the modeled lockstep block (Fig. 2 and 3) and (col. 2, lines 51-56) and (col. 3, lines 12-22).

As per claim 10, Mandyam discloses a system for verifying core determinacy (Fig. 1), the system comprising:

means for determining if a modeled processor is operating in a lockstep mode (col. 13, lines 22-36)

means for extracting data stored in core model structures (col. 6, lines 57-65)

means for comparing the extracted data to determine if any data associated with one processor core does not match data associated with another processor core (Fig. 1, element 110)

means for determining if any mismatching data will cause core divergence (col. 9, lines 14-16) and (Figs. 10A-10C).

Please refer to claim 1 for response to amendments.

As per claim 11, Mandyam discloses the means for determining if the modeled processor is operating in a lockstep mode comprise means for analyzing at least one of a modeled lockstep block and a lockstep block checker (col. 12, lines 57-67).

Safford et al. teaches:

the modeled lockstep block being configured to monitor operation of the modeled processor cores and the, lockstep block checker being configured to monitor operation of the modeled lockstep block (Fig. 2 and 3) and (col. 2, lines 51-56) and (col. 3, lines 12-22).

As per claim 12, Mandyam discloses means for extracting data comprise means for extracting data from core data storage and interconnect elements (col. 8, lines 15-20).

As per claim 13, Mandyam discloses means for determining if any mismatching data will cause core divergence comprise at least one of a data structure (col. 6, lines 57-65) and an algorithm (col. 10, lines 33-40).

As per claim 14, Mandyam discloses means for pending a check (Fig. 13, BNE SYNC _ERROR) for a lockstep block checker to signal when divergence occurs (col. 12, lines 57-67).

Safford et al. teaches:

the lockstep block checker being configured to monitor operation of a modeled lockstep block of the modeled single processor, the modeled lockstep block being configured to monitor operation of the modeled processor cores (Fig. 2 and 3) and (col. 2, lines 51-56) and (col. 3, lines 12-22).

As per claim 15, Mandyam discloses means for flagging an error (col. 9, lines 14-16) and (col. 8, lines 30-45).

As per claim 16, Mandyam discloses a determinacy checker (Fig. 1, element 106), stored on a computer-readable medium (Fig. 1) the system comprising:

logic configured to determine if a modeled processor is operating in a lockstep mode (col. 13, lines 22-36)

logic configured to extract data stored in core model structures (col. 6, lines 57-65)

logic configured to compare the extracted data (Fig. 1, element 110)

logic configured to determine if any data associated with one processor core does not match data associated with another processor core (Fig. 12) and (col. 13, lines 22-36)

logic configured to determine if any mismatching data will cause core divergence (col. 13, lines 22-36)

logic configured to facilitate notification of an error if any mismatching data will cause core divergence (col. 9, lines 14-16) and (Figs. 10A-10C).

Please refer to claim 1 for response to amendments.

As per claim 17, Mandyam discloses logic configured to determine if the modeled single processor is operating in a lockstep mode comprises logic configured to analyze at least one of a modeled lockstep block and a lockstep block checker (Fig. 16).

Safford et al. teaches:

the modeled lockstep block being configured to monitor operation of the modeled processor cores and the, lockstep block checker being configured to monitor operation of the modeled lockstep block (Fig. 2 and 3) and (col. 2, lines 51-56) and (col. 3, lines 12-22).

As per claim 18, Mandyam discloses logic configured to extract data comprises logic configured to extract data from core data storage and interconnect elements (col. 8, lines 15-20).

As per claim 19, Mandyam discloses logic configured to determine if any mismatching data will cause core divergence (col. 13, lines 22-36) comprises logic configured to access at least one of a data structure that matches divergence results with given mismatched data (col. 6, lines 57-65) and an algorithm that uses the mismatched data as inputs (col. 10, lines 33-40).

As per claim 20, Mandyam discloses logic configured to facilitate notification comprises logic configured to pend a check (Fig. 13, BNESYNC _ERROR) for a lockstep block checker to signal when divergence occurs (col. 12, lines 57-67).

Safford et al. teaches:

the lockstep block checker being configured to monitor operation of a modeled lockstep block of the modeled single processor, the modeled lockstep block being configured to monitor operation of the modeled processor cores (Fig. 2 and 3) and (col. 2, lines 51-56) and (col. 3, lines 12-22).

As per claim 21, Mandyam discloses the logic configured to facilitate notification comprises logic configured to flag an error (col. 9, lines 14-16) and (col. 8, lines 30-45).

As per claim 22, Mandyam discloses a computer system (Fig. 1), comprising:

a processing device (Fig. 2A, elements P0, P1)

and memory (Fig. 1) including a determinacy checker (Fig. 1, element 106) that is configured to extract data stored in core model structures (col. 6, lines 57-65) compare the extracted data (Fig. 1, element 110), determine if any mismatching data will cause core divergence (col. 13, lines 22-36)

and facilitate notification of an error if the mismatching data will cause core divergence (col. 9, lines 14-16) and (Figs. 10A-10C).

Please refer to claim 1 for response to amendments.

As per claim 23, Mandyam discloses checker is configured to extract data from core data storage and interconnect elements (col. 8, lines 15-20).

As per claim 24, Mandyam discloses checker is configured to pend a check (Fig. 13, BNE SYNC _ERROR) for a lockstep block checker to signal when divergence occurs (col. 12, lines 57-67).

Safford et al. teaches:

the lockstep block checker being configured to monitor operation of a modeled lockstep block of the modeled single processor, the modeled lockstep block being configured to monitor operation of the modeled processor cores (Fig. 2 and 3) and (col. 2, lines 51-56) and (col. 3, lines 12-22).

As per claim 25, Mandyam discloses checker is configured to flag an error (col. 9, lines 14-16) and (col. 8, lines 30-45).

Response to Arguments

Applicant's arguments have been fully considered with the examiner's response detailed below. Applicant's arguments see pages 9-11, filed October 23, 2006 with respect to the rejection(s) of claim(s) 1-25 under 35 USC § 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made over Mandyam et al. (U.S. Patent No. 5,928,334) in view of Safford et al. (U.S. Patent No. 7,003,691). Refer to the corresponding section of the claim analysis for details.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1 .136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1 .136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).